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APPLICATION NO.	FILING DATE	FIRST NAMED INVENTOR	ATTORNEY DOCKET NO.	CONFIRMATION NO.
10/071,689	02/08/2002	Zhong Dong	M-12327 US	2077

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EXAMINER	
PIZARRO CRESPO, MARCOS D	
ART UNIT	PAPER NUMBER
2814	

DATE MAILED: 11/05/2003

Please find below and/or attached an Office communication concerning this application or proceeding.

Office Action Summary	Application No.	Applicant(s)	
	10/071,689	DONG ET AL.	
	Examiner	Art Unit	
	Marcos D. Pizarro-Crespo	2814	

-- The MAILING DATE of this communication appears on the cover sheet with the correspondence address --

Period for Reply

A SHORTENED STATUTORY PERIOD FOR REPLY IS SET TO EXPIRE 3 MONTH(S) FROM THE MAILING DATE OF THIS COMMUNICATION.

- Extensions of time may be available under the provisions of 37 CFR 1.136(a). In no event, however, may a reply be timely filed after SIX (6) MONTHS from the mailing date of this communication.
- If the period for reply specified above is less than thirty (30) days, a reply within the statutory minimum of thirty (30) days will be considered timely.
- If NO period for reply is specified above, the maximum statutory period will apply and will expire SIX (6) MONTHS from the mailing date of this communication.
- Failure to reply within the set or extended period for reply will, by statute, cause the application to become ABANDONED (35 U.S.C. § 133).
- Any reply received by the Office later than three months after the mailing date of this communication, even if timely filed, may reduce any earned patent term adjustment. See 37 CFR 1.704(b).

Status

1)☒ Responsive to communication(s) filed on *25 July 2003* .

2a)☒ This action is **FINAL**. 2b)☐ This action is non-final.

3)☐ Since this application is in condition for allowance except for formal matters, prosecution as to the merits is closed in accordance with the practice under *Ex parte Quayle*, 1935 C.D. 11, 453 O.G. 213.

Disposition of Claims

4)☒ Claim(s) *17,20-28 and 30-35* is/are pending in the application.

4a) Of the above claim(s) _____ is/are withdrawn from consideration.

5)☐ Claim(s) _____ is/are allowed.

6)☒ Claim(s) *17,20-28,30-35* is/are rejected.

7)☐ Claim(s) _____ is/are objected to.

8)☐ Claim(s) _____ are subject to restriction and/or election requirement.

Application Papers

9)☐ The specification is objected to by the Examiner.

10)☐ The drawing(s) filed on _____ is/are: a)☐ accepted or b)☐ objected to by the Examiner.

Applicant may not request that any objection to the drawing(s) be held in abeyance. See 37 CFR 1.85(a).

11)☐ The proposed drawing correction filed on _____ is: a)☐ approved b)☐ disapproved by the Examiner.

If approved, corrected drawings are required in reply to this Office action.

12)☐ The oath or declaration is objected to by the Examiner.

Priority under 35 U.S.C. §§ 119 and 120

13)☐ Acknowledgment is made of a claim for foreign priority under 35 U.S.C. § 119(a)-(d) or (f).

a)☐ All b)☐ Some * c)☐ None of:

1.☐ Certified copies of the priority documents have been received.

2.☐ Certified copies of the priority documents have been received in Application No. _____ .

3.☐ Copies of the certified copies of the priority documents have been received in this National Stage application from the International Bureau (PCT Rule 17.2(a)).

* See the attached detailed Office action for a list of the certified copies not received.

14)☐ Acknowledgment is made of a claim for domestic priority under 35 U.S.C. § 119(e) (to a provisional application).

a) ☐ The translation of the foreign language provisional application has been received.

15)☐ Acknowledgment is made of a claim for domestic priority under 35 U.S.C. §§ 120 and/or 121.

Attachment(s)

1) ☐ Notice of References Cited (PTO-892)
2) ☐ Notice of Draftsperson's Patent Drawing Review (PTO-948)
3) ☐ Information Disclosure Statement(s) (PTO-1449) Paper No(s) _____ .
4) ☐ Interview Summary (PTO-413) Paper No(s). _____ .
5) ☐ Notice of Informal Patent Application (PTO-152)
6) ☐ Other: .

Attorney's Docket Number: M-12327 US
Filing Date: 2/8/2002
Claimed Foreign Priority Date: none
Applicant(s): Dong et al.
Examiner: Marcos D. Pizarro-Crespo

DETAILED ACTION

This Office action responds to the reply filed on 7/25/2003.

Acknowledgment

1. The reply filed on 7/25/2003 in response to the Office action mailed on 5/7/2003 has been entered. The present Office action is made with all the suggested amendments being fully considered. Accordingly, pending in this Office action are claims 17, 20-28, and 30-35.

Claim Rejections - 35 USC § 103

2. The following is a quotation of 35 U.S.C. 103(a) which forms the basis for all obviousness rejections set forth in this Office action:

> (a) A patent may not be obtained though the invention is not identically disclosed or described as set forth in section 102 of this title, if the differences between the subject matter sought to be patented and the prior art are such that the subject matter as a whole would have been obvious at the time the invention was made to a person having ordinary skill in the art to which said subject matter pertains. Patentability shall not be negatived by the manner in which the invention was made.

3. This application currently names joint inventors. In considering patentability of the claims under 35 U.S.C. 103(a), the examiner presumes that the subject matter of the various claims was commonly owned at the time any inventions covered therein were made absent any evidence to the contrary. Applicant is advised of the obligation under 37 CFR 1.56 to point out the inventor and invention dates of each claim that was

not commonly owned at the time a later invention was made in order for the examiner to consider the applicability of 35 U.S.C. 103(c) and potential 35 U.S.C. 102(e), (f) or (g) prior art under 35 U.S.C. 103(a).

4. Claims 17, 21-25, and 27 are rejected under 35 U.S.C. 103(a) as being unpatentable over Hagiwara (US 5847427) in view of Misium (US 6261973) and George (US 6140024).

5. Hagiwara shows most aspects of the instant invention including a method of manufacturing an integrated circuit comprising a nonvolatile memory, the method comprising:

- forming a first layer **202** comprising a silicon surface, the first layer providing one floating gate for the memory (see, *e.g.*, fig. 10A)
- nitriding the silicon surface of the first layer **202** to incorporate nitrogen atoms into the silicon surface (see, *e.g.*, fig. 10C)
- forming a first dielectric **203** at the nitrided surface **222**, wherein forming the first dielectric **203** comprises forming silicon oxide at the nitrided surface **222** (see, *e.g.*, fig. 10C and col.7/ll.42-58)
- forming a conductive layer **204** separated from the nitrided surface **222** by the first dielectric **203**, the conductive layer **204** providing one control gate for the memory (see, *e.g.*, fig. 10E)

Hagiwara (see, *e.g.*, col.7/ll.59-67) also teaches that ion implantation may be used during the nitriding step to incorporate nitrogen atoms into the silicon surface, but fails to specify the use of remote plasma nitridation (RPN).

Misium (see, *e.g.*, col.2/ll.1-3), on the other hand, teaches that RPN is an improved low-temperature ion-implantation method for creating a nitrided layer. This method will also help to prevent device failure due to the mechanical stress that occurs within nitride layers during high-temperature processing-steps (see, *e.g.*, col.1/ll.63-67). In addition, Misium teaches that RPN may be used during the nitridation step of either an oxide layer (see, *e.g.*, figs. 1C and 2B) or a silicon surface (see, *e.g.*, fig. 3C).

Like Misium, George (see, *e.g.*, col.2/ll.21-33) teaches that using RPN for nitriding an oxide layer will help lessen the usual stress associated within nitride layers while providing for a low-temperature nitriding step. George additionally teaches that RPN may also be used to protect the silicon surface of Hagiwara's first layer and that doing so will improve the device reliability (see, *e.g.*, George/col.5/ll.62-col.6/ll.2).

It would have been obvious at the time of the invention to one of ordinary skill in the art to nitride Hagiwara's silicon surface by RPN, as suggested by Misium and George, to lower the thermal budget of the process and improve the device reliability.

6. Regarding claim 21, Hagiwara (see, *e.g.*, col.5/ll.59) shows that the silicon surface is a polysilicon surface.

7. Regarding claim 22, Hagiwara shows the forming the first dielectric further comprises:

- forming the first dielectric **203** to have a silicon oxide surface (see, *e.g.*, col.7/ll.42-58)
- nitriding the silicon oxide surface of the first dielectric to incorporate nitrogen atoms into the silicon oxide surface (see, *e.g.*, col.7/ll.42-58)

8. Regarding claim 23, Hagiwara (col.7/ll.59-62) shows that nitriding the silicon oxide surface may comprise ion implantation of a material comprising nitrogen into the silicon oxide surface.

9. Regarding claim 24, Misium shows that nitriding the silicon oxide surface comprises generating a plasma of nitrogen ions, and exposing the silicon oxide surface to the plasma (see, *e.g.*, col.2/ll.48-63).

10. Regarding claim 25, Hagiwara teaches (see, *e.g.*, col.7/ll.59-67) that ion implantation may be used during the nitriding step to incorporate nitrogen atoms into the silicon oxide surface. Misium (see, *e.g.*, col.2/ll.1-3), on the other hand, teaches that RPN is an improved low-temperature process that could be used during Hagiwara's ion-implantation step to create a nitrided layer that is resistant to oxide etchants.

11. Regarding claim 27, Hagiwara/Misium/George shows most aspects of the instant invention (see paragraphs 5-10 above), except for the step of nitriding the silicon oxide surface resulting in a nitrided silicon oxide layer less than 3 nm thick. Hagiwara (see, *e.g.*, col.6/ll.11), however, shows that an illustrative thickness for such a layer may fall between 5 to 10 nm. Misium (see, *e.g.*, col.4/ll.41-52), on the other hand, teaches that varying the thickness of the nitrided silicon oxide layer would have been within the knowledge of those having ordinary skill in the art.

Besides the teachings in the prior art, it has been held that a *prima facie* case of obviousness exists where the claimed values and the prior art ranges do not overlap but are close enough that one skilled in the art would have expected them to have the same properties.

It appears that the differences in thickness between the claimed layer and that of Hagiwara/Misium/George does not change the properties of the layer and therefore would have been obvious (*Titanium Metals Corp of America v. Banner*, 778 F.ed 775, 227 USPQ 773 (Fed. Cir. 1985)).

12. Claims 26 is rejected under 35 U.S.C. 103(a) as being unpatentable over Hagiwara/Misium/George and Furukawa (US 2002/0185675).

13. Hagiwara/Misium/George shows most aspects of the instant invention (see paragraphs 5-11 above). Misium and George, for example, use RPN during the step of nitriding the surface of the oxide layer, but fail to teach the use of decoupled plasma nitridation (DPN). Furukawa (see, *e.g.*, [par 0025]), on the other hand, teaches that DPN is an alternative technique to the use of RPN during the step of nitriding the silicon oxide surface of Hagiwara/Misium/George.

It would have been obvious at the time of the invention to use either DPN or RPN during the nitridation step of Hagiwara/Misium/George since the use in the semiconductor art and the selection of any of these known equivalent techniques, as taught by Furukawa, would be within the level of ordinary skill in the art.

14. Claims 17, 20, 28, and 30-35 are rejected under 35 U.S.C. 103(a) as being unpatentable over Lin (US 6127227) in view of Misium and George.

15. Lin shows most aspects of the instant invention including a method for manufacturing an integrated circuit comprising a nonvolatile memory, the method comprising:

- forming a first layer **120** comprising a silicon surface, the first layer providing a floating gate for the memory (see, *e.g.*, fig. 2B)
- nitriding the silicon surface of the first layer **120** to incorporate nitrogen atoms into the silicon surface (see, *e.g.*, fig. 2B)
- forming a first dielectric **143** at the nitrided surface, wherein forming the first dielectric **143** comprises forming silicon oxide at the nitrided surface (see, *e.g.*, fig. 2C)
- forming a conductive layer **150** separated from the nitrided surface by the first dielectric **143**, the conductive layer **150** providing a control gate for the memory

Lin (see, *e.g.*, col.4/ll.42-46) also teaches that ion implantation may be used during the nitriding step to incorporate nitrogen atoms into the silicon surface, but fails to specify the use of RPN.

Misium (see, *e.g.*, col.2/ll.1-3), on the other hand, teaches that RPN is an improved low-temperature ion-implantation step that can be used for creating Lin's nitrided layer. This method step will help prevent device failure due to the mechanical stress occurring within nitride layers during high-temperature processing-steps (see, *e.g.*, col.1/ll.63-67). In addition, Misium teaches that RPN may be used during the nitridation step of either an oxide layer (see, *e.g.*, figs. 1C and 2B) or a silicon surface (see, *e.g.*, fig. 3C).

Likewise, George (see, *e.g.*, col.2/ll.21-33) teaches that using RPN for nitriding an oxide layer will help lessen the usual stress associated with nitride layers while

providing for a low-temperature nitriding step. George further teaches that RPN may also be used to protect the silicon surface of Lin's first layer (see, *e.g.*, George/col.5/ll.62-67). Doing so will improve the device reliability (see, *e.g.*, George/col.5/ll.67-col.6/ll.2).

It would have been obvious at the time of the invention to one of ordinary skill in the art to nitride Lin's silicon surface by remote plasma nitridation, as suggested by Misium and George, to lower the thermal budget of the process and improve the device reliability.

16. Regarding claim 20, Lin (see, *e.g.*, col.4/ll.60) shows that forming the silicon oxide at the nitrided surface comprises forming the silicon oxide by thermal oxidation.

17. Regarding claim 28, Lin (see, *e.g.*, col.4/ll.66) shows that nitriding the silicon surface results in forming at the silicon surface a layer of nitrided silicon less than 3 nm thick.

18. Regarding claim 30, Lin shows most aspects of the instant invention including a method for manufacturing an integrated circuit comprising a nonvolatile memory, the method comprising:

- forming a first polysilicon layer **120** to provide one or more floating gates of the nonvolatile memory (see, *e.g.*, fig. 2B)
- nitriding the surface of the first polysilicon layer **120** to incorporate nitrogen atoms into the surface (see, *e.g.*, fig. 2B)
- forming a first dielectric **143** at the nitrided surface (see, *e.g.*, fig. 2C)

- forming a conductive layer **150** separated from the nitrided surface by the first dielectric **143** (see, *e.g.*, fig. 2F)

wherein the step of forming the first dielectric comprises forming silicon oxide on the nitrided surface by thermal oxidation (see, *e.g.*, col.4/ll.58-61), the nitrogen atoms reduce the rate of growth of the silicon oxide on the nitrided surface (see, *e.g.*, col.4/ll.45-49), and the conductive layer provides one or more control gates for the memory (see, *e.g.*, fig. 2G).

19. Regarding claim 31, Misium (see, *e.g.*, col.4/ll.42) and George (see, *e.g.*, col.6/ll.64-66) teach that the RPN step may be performed at a temperature between 300-500°C.

20. Regarding claim 32, Misium (see, *e.g.*, figs. 3A-3C) shows that the first layer may be patterned before the RPN.

21. Regarding claim 33, Lin shows that the RPN step is a blanket process (see, *e.g.*, fig. 2B).

22. Regarding claims 34 and 35, Misium (see, *e.g.*, figs. 1A-1C) and George (see, *e.g.*, figs. 1A-1C) show that a mask may be used during the RPN step to block nitrogen from a region of the integrated circuit. Lin (see, *e.g.*, fig. 2G) shows that the first layer may be patterned after ion implanting nitrogen atoms into the first layer.

Response to Arguments

23. The applicants argue:

Hagiwara teaches away from the RPN by emphasizing the desirability of performing nitridation in a CVD device.

The examiner responds:

Hagiwara does not teach away from RPN by emphasizing the desirability of performing CVD nitridation. In fact, Hagiwara teaches that a preferred method to nitride the silicon surface is nitrogen implantation (see, *e.g.*, col.5/ll.46 and col.6/ll.4).

24. The applicants argue:

> Misium does not teach that his RPN device can be used for the interpoly insulation film deposition in Hagiwara. Moreover, Misium's RPN is directed to the RPN of silicon dioxide, not the RPN of silicon, as recited in claim 17. He incidentally discloses the RPN of silicon during the RPN of his silicon dioxide, but does not disclose any benefits of the silicon RPN.

The examiner responds:

Hagiwara (see, *e.g.*, col.5/ll.46 and col.7/ll.59-67) teaches that ion implantation is a preferred nitridation step that may be used to incorporate atoms into the silicon surface. Misium (see, *e.g.*, col.2/ll.1-3), on the other hand, teaches that RPN is an improved low-temperature ion implantation method for creating a nitrided layer. Additionally, Misium (see, *e.g.*, col.1/ll.63-67) teaches that RPN reduce the mechanical stress within nitride layers. This may prevent device failures caused by the mechanical stress that occurs within nitride layers during high-temperature processing steps.

It would have been obvious at the time of the invention to one of ordinary skill in the art to use RPN for the ion implantation step of Hagiwara, as suggested by Misium, to lower the thermal budget of the process and improve the device reliability.

25. The applicants argue:

> George is concerned with protecting the silicon wafer from contamination during resist stripping. The silicon wafer 10 is protected performing RPN of an oxide layer 12. This prevents the exposure of the wafer to contaminants from the photoresist layer during the step of stripping the photoresist (see, *e.g.*, col.4/ll.30-60). He, however, fails to teach the nitridation of silicon, as recited in claim 17.

The examiner responds:

Hagiwara (see, *e.g.*, col.5/ll.46 and col.7/ll.59-67) teaches that ion implantation is a preferred nitridation step that may be used to incorporate atoms into a silicon surface. Misium (see, *e.g.*, col.2/ll.1-3), on the other hand, teaches that RPN is an improved low-temperature ion implantation method for creating a nitrided layer. Additionally, Misium (see, *e.g.*, col.1/ll.63-67) teaches that RPN reduce the mechanical stress within nitride layers. This may prevent device failures caused by the mechanical stress that occurs within nitride layers during high-temperature processing steps.

Likewise, George (see, *e.g.*, col.2/ll.22-25) teaches that RPN is an improved low-temperature ion implantation method for creating a nitrided layer. He also teaches that RPN lessens the mechanical stress within nitride layers (see, *e.g.*, col.2/ll.26-30). George further teaches that RPN forms a nitrided surface that is an effective barrier against mobile ions, which tend to decrease device reliability.

It would have been obvious at the time of the invention to one of ordinary skill in the art to use RPN for the ion implantation step of Hagiwara, as suggested by Misium and George, to lower the thermal budget of the process and improve the device reliability.

Conclusion

26. **THIS ACTION IS MADE FINAL.** Applicant is reminded of the extension of time policy as set forth in 37 CFR 1.136(a).

27. A shortened statutory period for reply to this final action is set to expire THREE MONTHS from the mailing date of this action. In the event a first reply is filed within TWO MONTHS of the mailing date of this final action and the advisory action is not

mailed until after the end of the THREE-MONTH shortened statutory period, then the shortened statutory period will expire on the date the advisory action is mailed, and any extension fee pursuant to 37 CFR 1.136(a) will be calculated from the mailing date of the advisory action. In no event, however, will the statutory period for reply expire later than SIX MONTHS from the mailing date of this final action.

28. Papers related to this application may be submitted directly to Art Unit 2814 by facsimile transmission. Papers should be faxed to Art Unit 2814 via the Art Unit 2814 Fax Center located in Crystal Plaza 4, room 3C23. The faxing of such papers must conform to the notice published in the Official Gazette, 1096 OG 30 (15 November 1989). The Art Unit 2814 Fax Center number is **(703) 308-7722** or **–7724**. The Art Unit 2814 Fax Center is to be used only for papers related to Art Unit 2814 applications.

29. Any inquiry concerning this communication or earlier communications from the examiner should be directed to **Marcos D. Pizarro-Crespo** at **(703) 308-6558** and between the hours of 9:30 AM to 8:00 PM (Eastern Standard Time) Monday through Thursday or by e-mail via Marcos.Pizarro@uspto.gov. If attempts to reach the examiner by telephone are unsuccessful, the examiner's supervisor, Wael Fahmy, can be reached on (703) 308-4918.

30. Any inquiry of a general nature or relating to the status of this application should be directed to the **Group 2800 Receptionist** at **(703) 308-0956**.

31. The following list is the Examiner's field of search for the present Office Action:

Field of Search	Date
U.S. Class / Subclass(es): 438/257-267,514-534, 257/324	10/29/2003
Other Documentation: PLUS Analysis	8/8/2002
Electronic Database(s): EAST (USPAT, EPO, JPO)	10/29/2003

LONG PHAM
PRIMARY EXAMINER

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MDP/mdp
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